METHOD OF REDUCING NOTCHING DURING REACTIVE ION ETCHING

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of reducing notching during reactive ion etching (RIE), and more particularly, to a method of reducing notching in a lower portion of a silicon layer when RIE is performed to pass through the silicon layer on a sequentially-stacked structure of the silicon layer, an insulating layer and a silicon substrate.

2. Description of the Related Art

A reactive ion etching (RIE) method has been generally used to pattern a silicon structure. However, when RIE is performed to pass through a silicon layer on a multi-layered structure of the silicon layer, an insulating layer and a silicon substrate, the silicon layer is prone to be overetched due to a microloading effect. For instance, as shown in FIG. 1, a region having a large aperture 36 in which the etching rate is fast is overetched while a region having a small aperture 34 in which the etching rate is slow is etched to be passed through. As a result, the surface of an insulating layer 20 is charged with electricity by an etching ion which reacts to form an electric potential on the insulating layer 20. Due to the electric potential, the etching ion is reflected from the insulating layer 20, which causes unnecessary lateral etching in a lower portion of a silicon layer 30. The lateral etching, i.e., notching 32, makes a structure thinner and further, the surface of the structure irregular, thereby deteriorating the mechanical and electrical characteristics.

To prevent such notching, there was an attempt to form a metal layer on an insulating layer so that an etching ion can be discharged therefrom. However, this method is inconvenient because it requires additional deposition of a metal layer and anodic bonding.

SUMMERY OF THE INVENTION

To solve the above problem, it is an object of the present invention to provide a method of remarkably reducing notching occurring in a lower portion of a silicon layer when RIE is performed to pass through the silicon layer on a

sequentially-stacked structure of the silicon layer, an insulating layer and a silicon substrate.

To accomplish the above object, there is provided a method of reducing notching occurring when RIE is performed to pass through a silicon layer in a multi-layered structure in which the silicon layer, an insulating layer and a silicon substrate are sequentially deposited according to the present invention. The method includes the steps of: (a) forming an insulating layer on a silicon substrate; (b) forming trenches on the insulating layer to expose the silicon substrate; (c) forming a silicon layer on the insulating layer to fill the trenches; and (d) patterning the silicon layer to form first etch regions, which pass through the silicon layer, to include the trenches.

It is preferable that in step (d) the silicon layer between the trenches is patterned to form second etch regions which are narrower than the first etch regions.

Also, it is preferable that in step (d) silicon filled in the trenches is removed to expose the silicon substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

The above objects and advantages of the present invention will become apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. 1 is a cross-sectional view of structure in which notching occurs according to conventional reactive-ion etching (RIE);

FIG. 2 is a perspective view of a structure according to a preferred embodiment of the present invention;

FIG. 3 is a cross-sectional view of the structure of FIG. 2, taken along the line III-III';

FIGS. 4A through 4E are cross-sectional views for explaining a method of reducing notching occurring during RIE according to a preferred embodiment of the present invention;

FIG. 5 is a photograph of a lower portion of a silicon layer after RIE is performed to pass through the silicon layer according to a conventional method, taken by a scanning electron microscope (SEM);

FIG. 6 is a SEM photograph of a lower portion of a silicon layer formed on an insulating layer having 3 μm-wide trenches after RIE is performed to pass through the silicon layer; and

FIG. 7 is a SEM photograph of a lower portion of a silicon layer formed on an insulating layer having 6 μm-wide trenches after RIE is performed to pass through the silicon layer.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 2 shows a perspective view of a multi-layered structure of a silicon layer, an insulating layer and a silicon substrate according to the present invention. FIG. 3 is a cross-sectional view of the multi-layered structure shown in FIG. 2, taken along the lines III-III'.

Referring to FIGS. 2 and 3, an insulating layer 200 having trenches 210 is formed on a silicon substrate 100 and a silicon layer 300 is formed on the insulating layer 200. The trenches 210 on the insulating layer 200 are positioned in respective etch regions 310 on the silicon layer 300.

FIGS. 4A through 4E are cross-sectional views for explaining a method of reducing notching occurring during RIE according to the present invention.

Referring to FIG. 4A, an insulating layer 200 is formed to a predetermined thickness on a silicon substrate 100. Next, the insulating layer 200 is patterned to form trenches 210 to pass through the insulating layer 200 as shown in FIG. 4B. As a result, the surface of the silicon substrate 100 placed below the trenches 210 is exposed. Then, as shown in FIG. 4C, a silicon layer 300 is formed on the insulating layer 200 to fill the trenches 210. Thereafter, RIE is performed on the silicon layer 300 (refer to FIG. 4D).

At this time, the etching rate in a region 306 having a large aperture is faster than that in a region 304 having a small aperture. Therefore, during RIE, the entire silicon layer 300 in the region 306 is etched to expose the surface of the insulating layer 200, whereas only a portion of the silicon layer 300 in the region 304 is etched.

Accordingly, if RIE is continued to etch the entire silicon layer 300 in the region 304, the silicon layer 300 filled in the trench 210 on the insulating layer 200, which is positioned below the large aperture 306, is etched to expose the silicon

substrate 100 as shown in FIG. 4E. At this time, etching ions are generated due to overetching in the region 306 and are discharged via the silicon substrate 100. Meanwhile, it is possible to omit a process of forming the trenches 210 on the insulating layer 200 below the region 304 having a small aperture when the regions 306 and 304 are etched together by RIE.

Experimental Example

FIG. 5 is a scanning electron microscope (SEM) photograph of a lower portion of a conventional silicon layer, which is formed on an insulating layer having no trenches and etched to be passed through by RIE. FIG. 6 is an SEM photograph of a lower portion of a silicon layer, which is formed on an insulating layer having 3 μm-wide trenches and etched to be passed through by RIE. FIG. 7 is an SEM photograph of a lower portion of a silicon layer, which is formed on an insulating layer having 6 μm-wide trenches and etched to be passed through by RIE.

In the experimental example, a silicon layer structure having a thickness of 52μm formed on a tetra ethylorthosilicate (TEOS) insulating layer having a thickness of 2.5 μm, was used. Firstly, silicon layers were formed on an insulating layer having no trenches, an insulating layer having 3 μm-wide trenches and an insulating layer having 6 μm-wide trenches, respectively. Then, when RIE was performed on the silicon layer to form an aperture of about 8 μm thereon, the silicon layer was deliberately about 30 % overetched to cause notching and the results are as shown in the SEM photographs in FIGS. 5 through 7.

Referring to FIG. 5, excessive notching occurred on the bottom of the silicon layer having no trenches due to the overetching. Referring to FIG. 6, a little notching occurred in a silicon layer on an insulating layer having 3 μm-wide trenches. However, from FIG. 7, it can be seen that notching was remarkably reduced in a silicon layer on an insulating layer having 6 μm-wide trenches. Usually, notching occurs in a lower portion of a wall of a silicon layer. Therefore, it seems that notching can be prevented by discharging etching ions near the lower portions of the walls, and further, the narrower a gap between the walls and the trenches is, the less the notching is.

As described above, in a method according to the present invention, it is possible to satisfactorily reduce notching without additional deposition of a metal

layer, when fabricating a multi-layered structure having a silicon layer which is etched to be passed through by RIE. Therefore, the method is very helpful in manufacturing a device requiring RIE.

While the present invention has been particularly shown and described with reference to the preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention as defined by the appended claims.